FIG.1A Block Diagram of Sequential Data Recovery

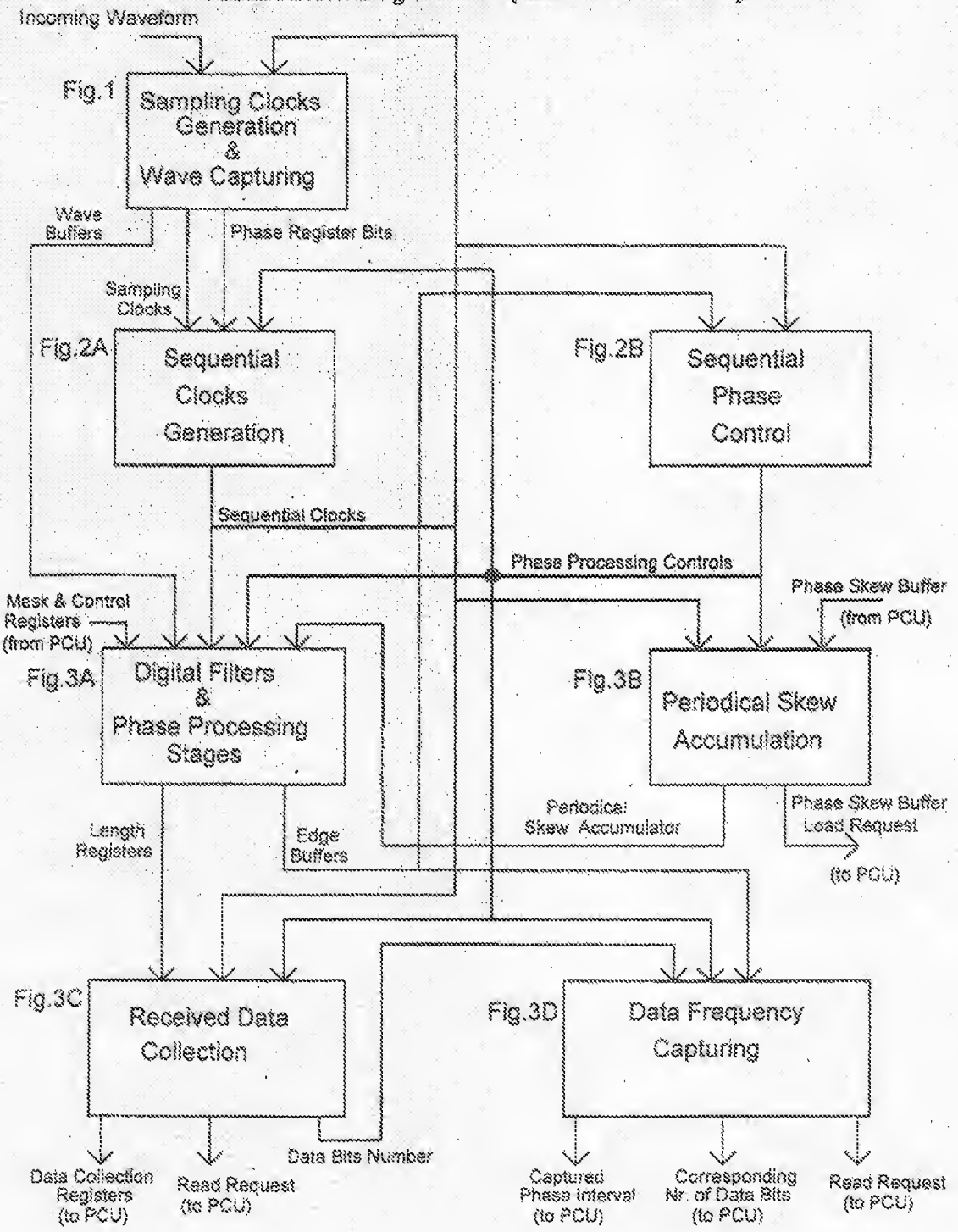


FIG.1 Sampling Clocks and Wave Capturing

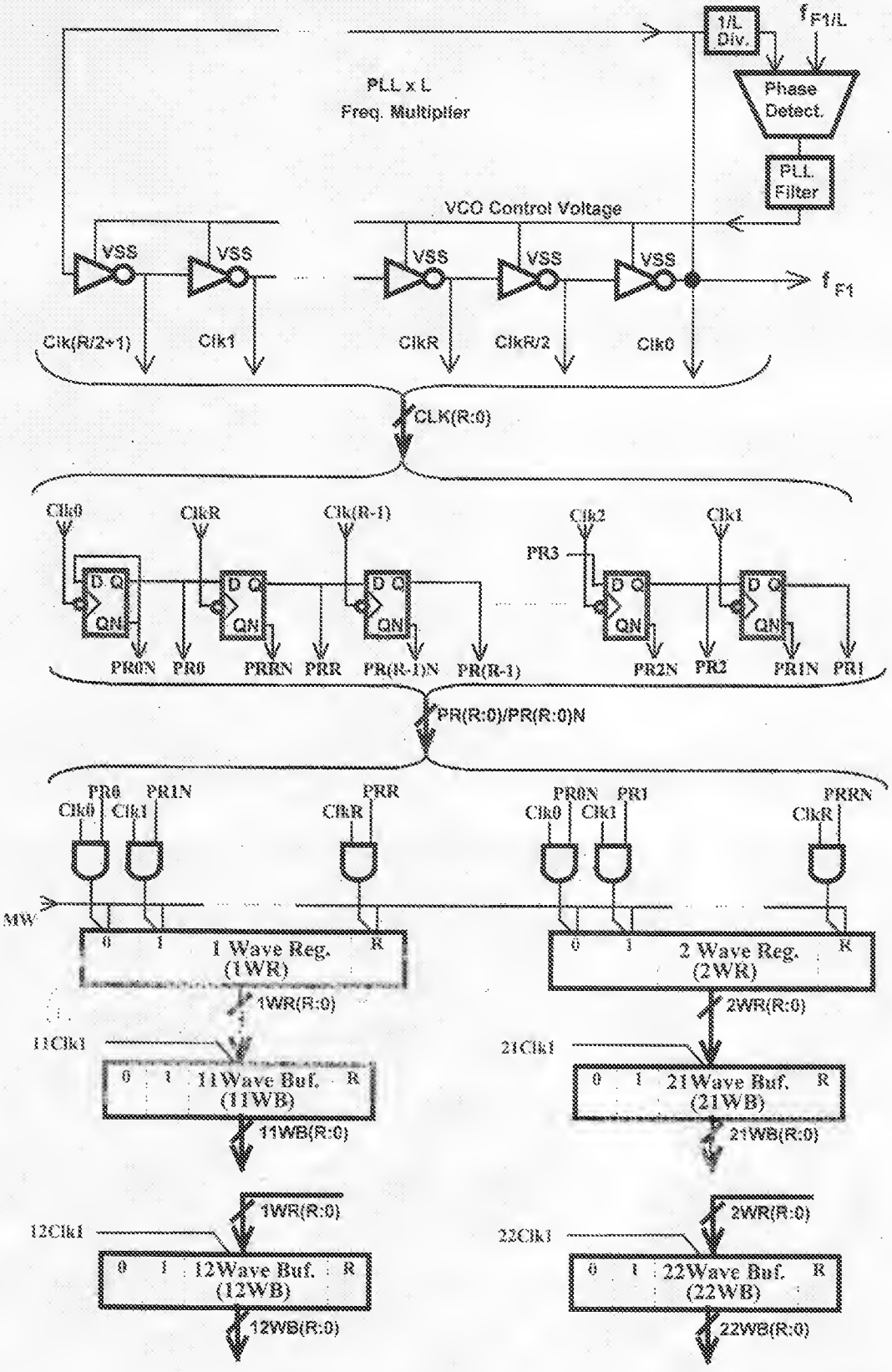


FIG.2A Sequential Clocks Generation (SCG)

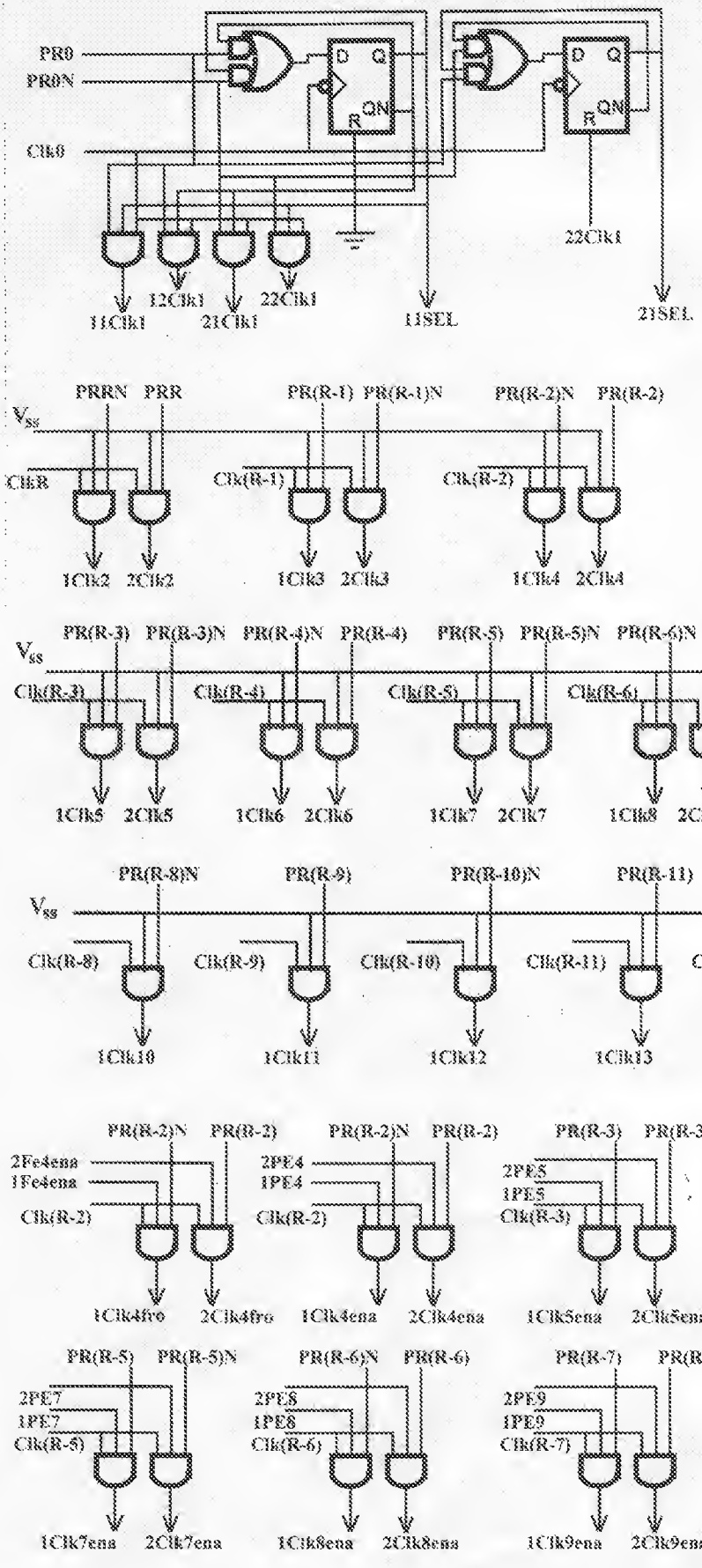


FIG.2B Sequential Phase Control (SPC)

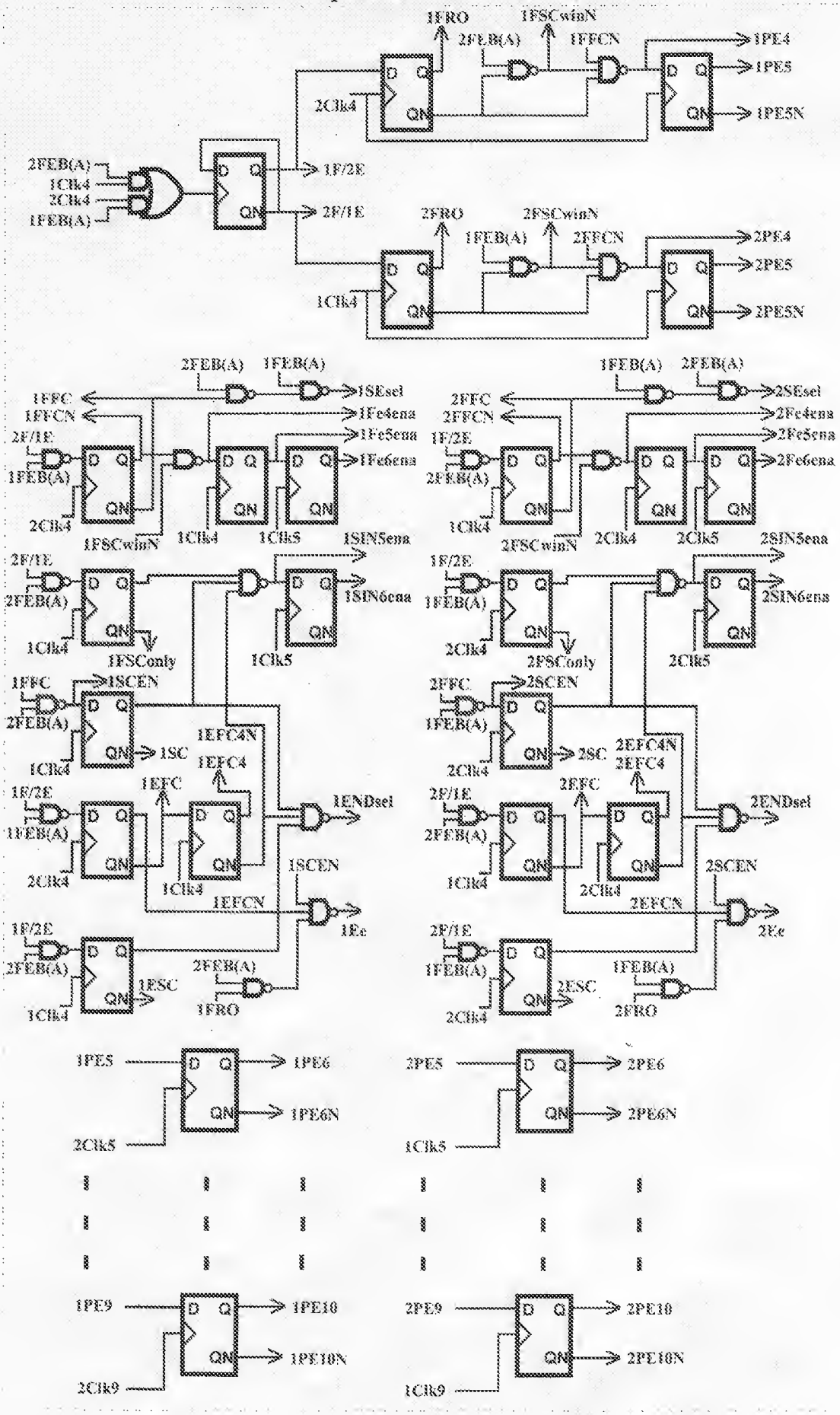


FIG.2C Timing Diagram of the SC and WC

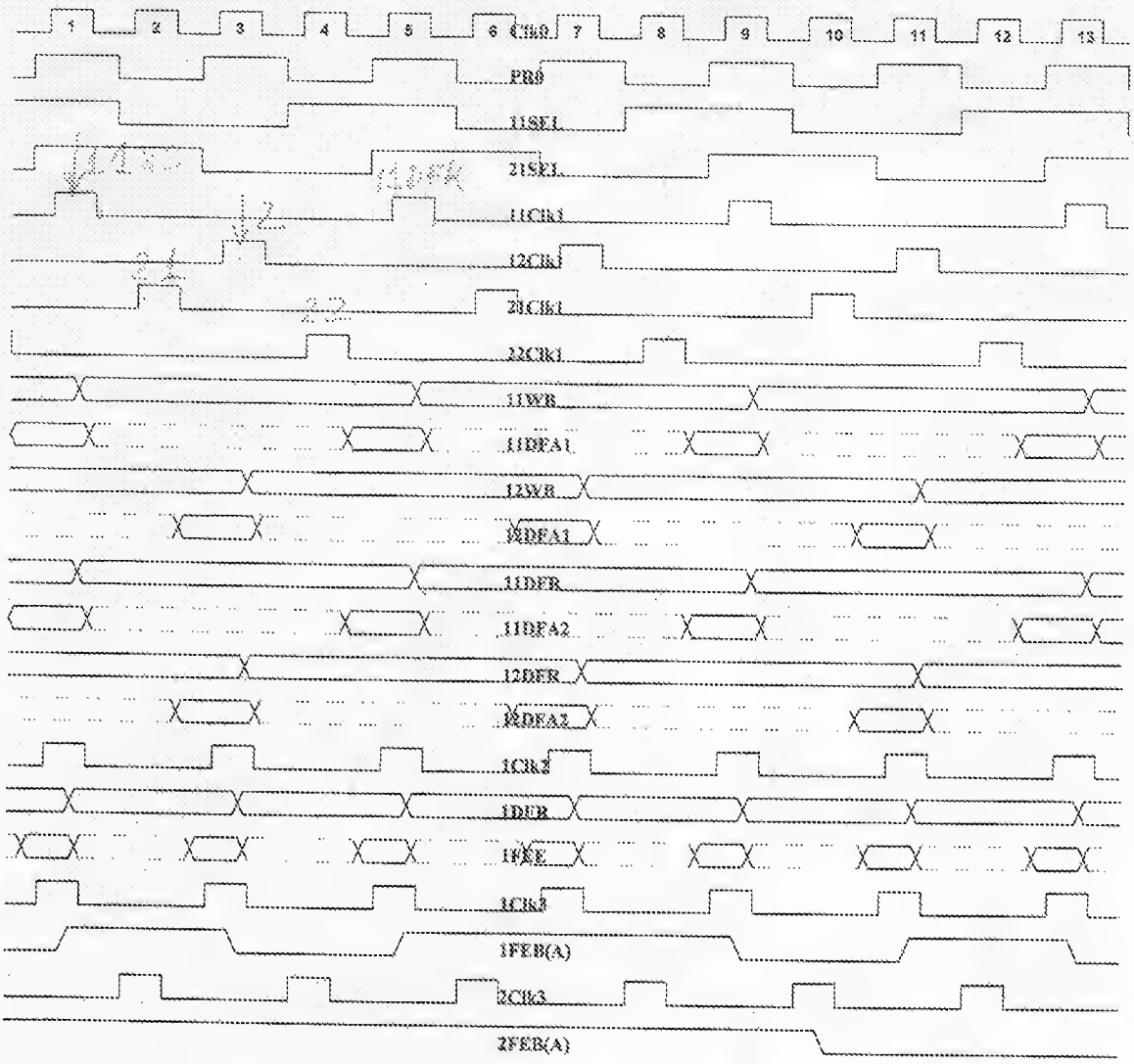


FIG.2D Timing Diagram of Sequential Phase Control proceeded by a phase2 long data string (continuation of FIG.2C)

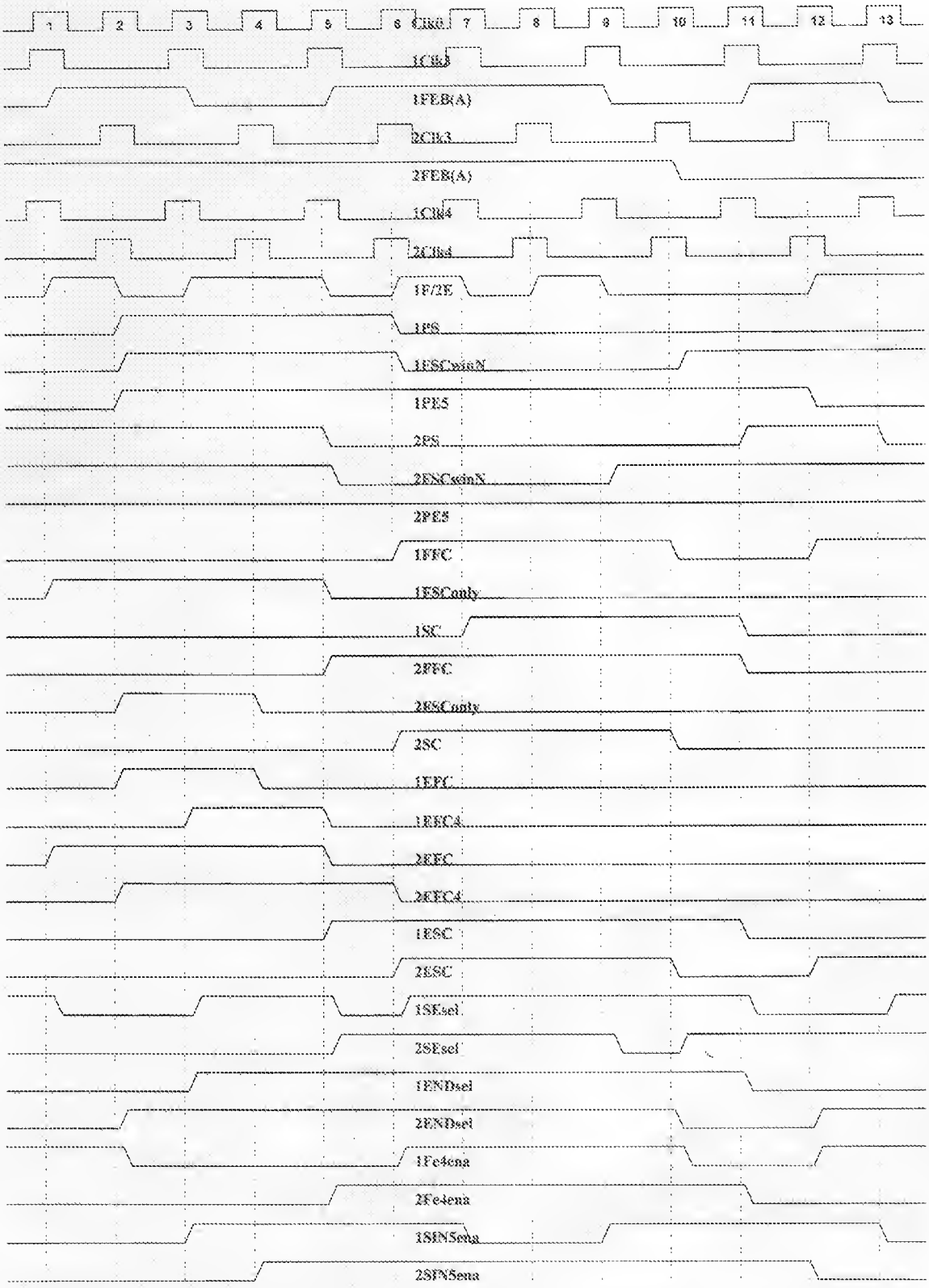


FIG.3A Phase1 of the Phase Processing Stages

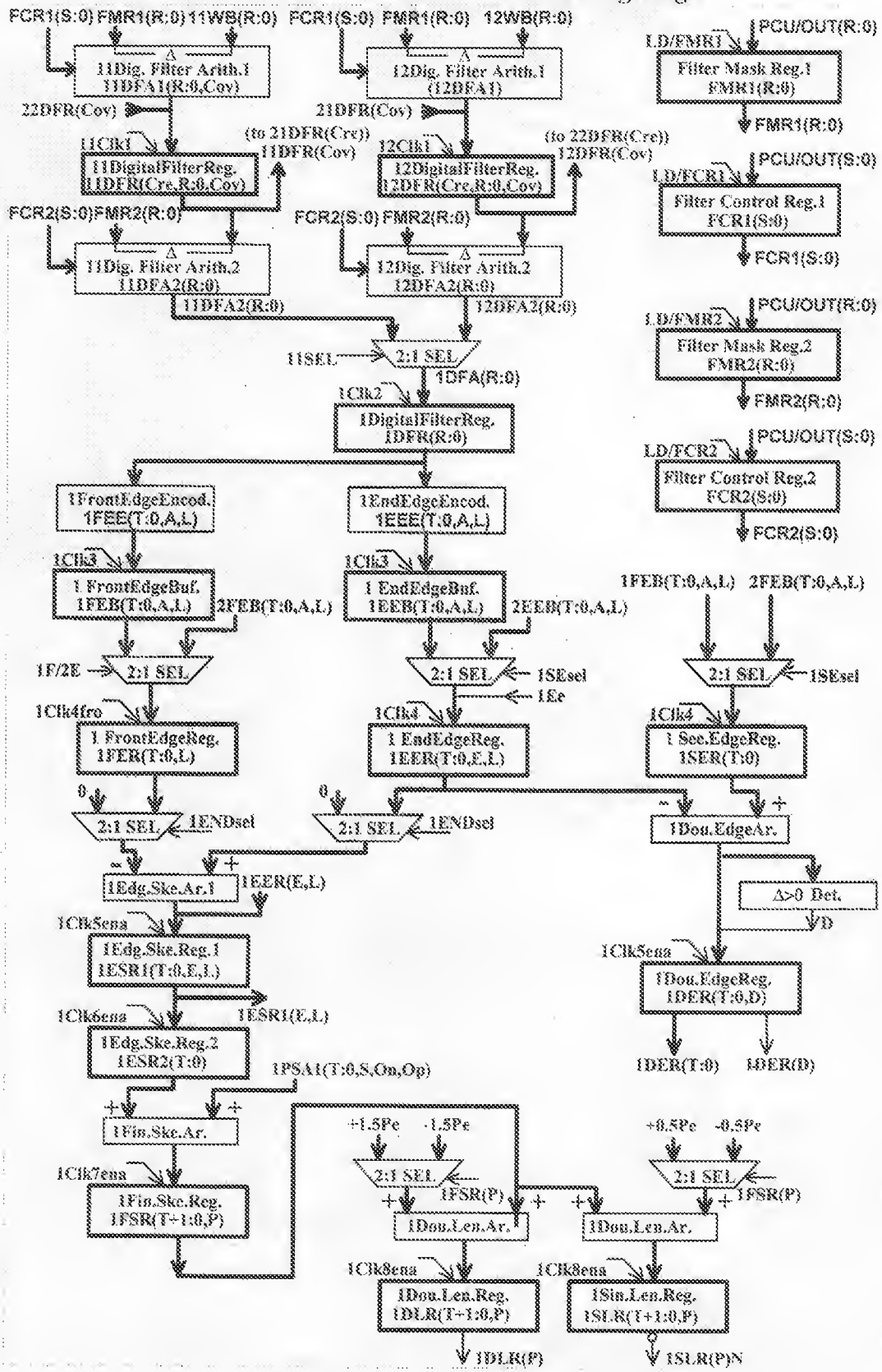


FIG.3B Periodical Skew Accumulation

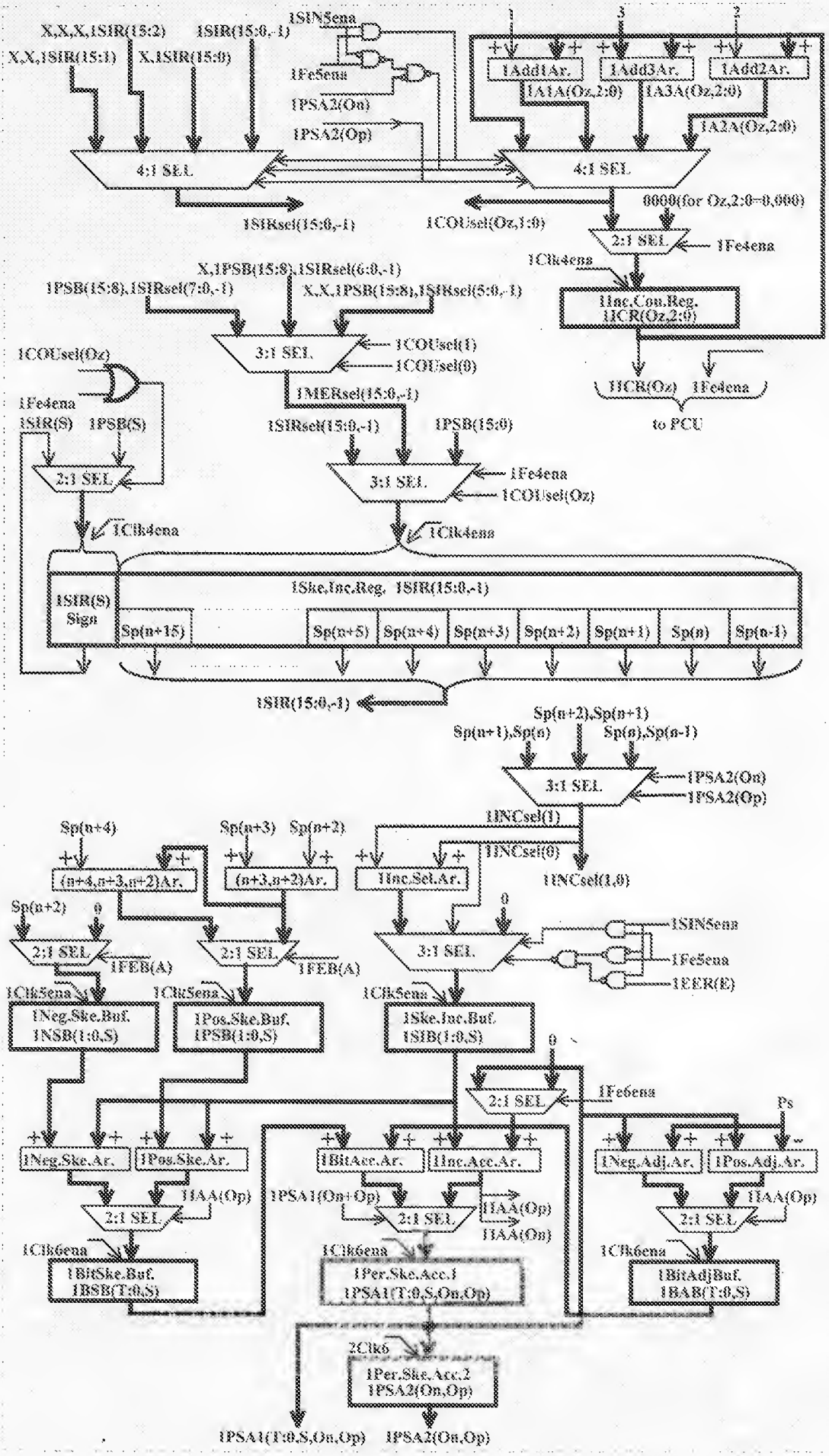
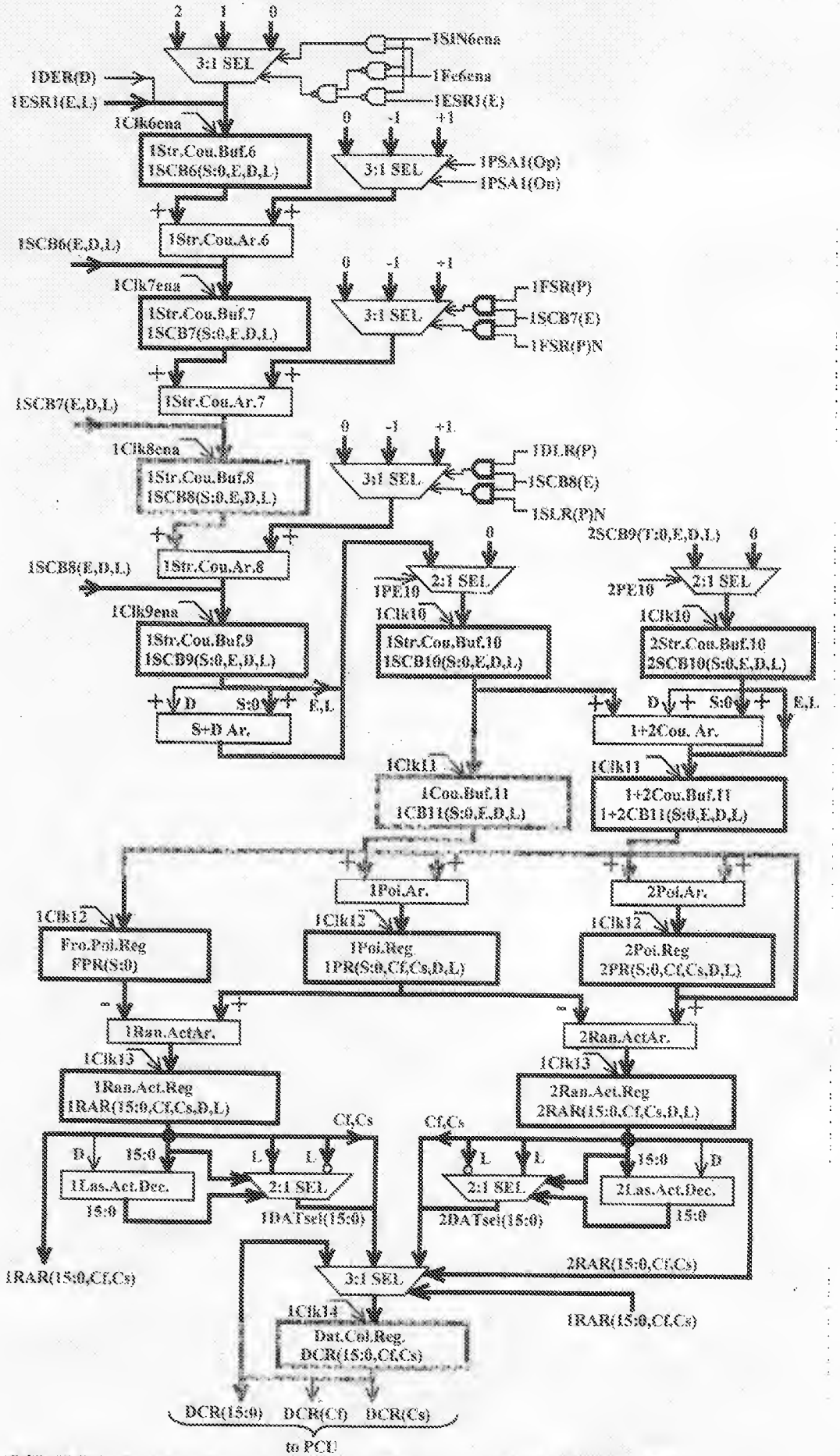
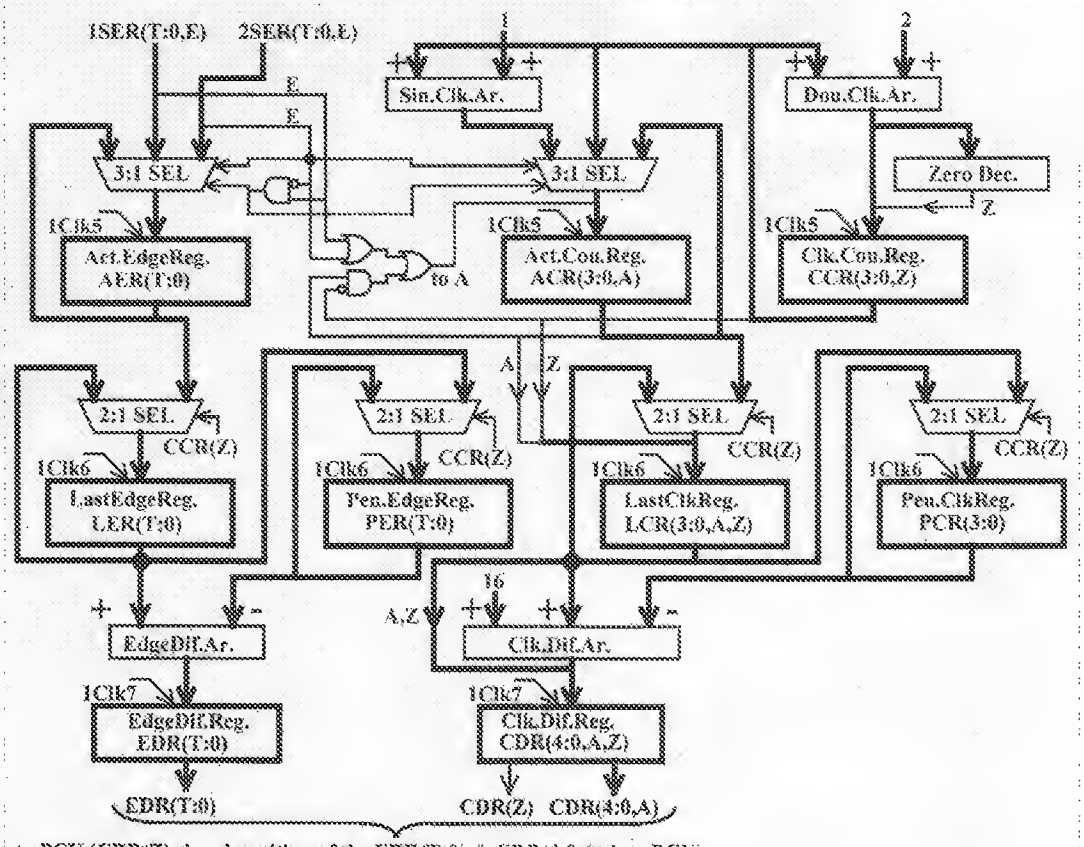


FIG.3C Received Data Collection

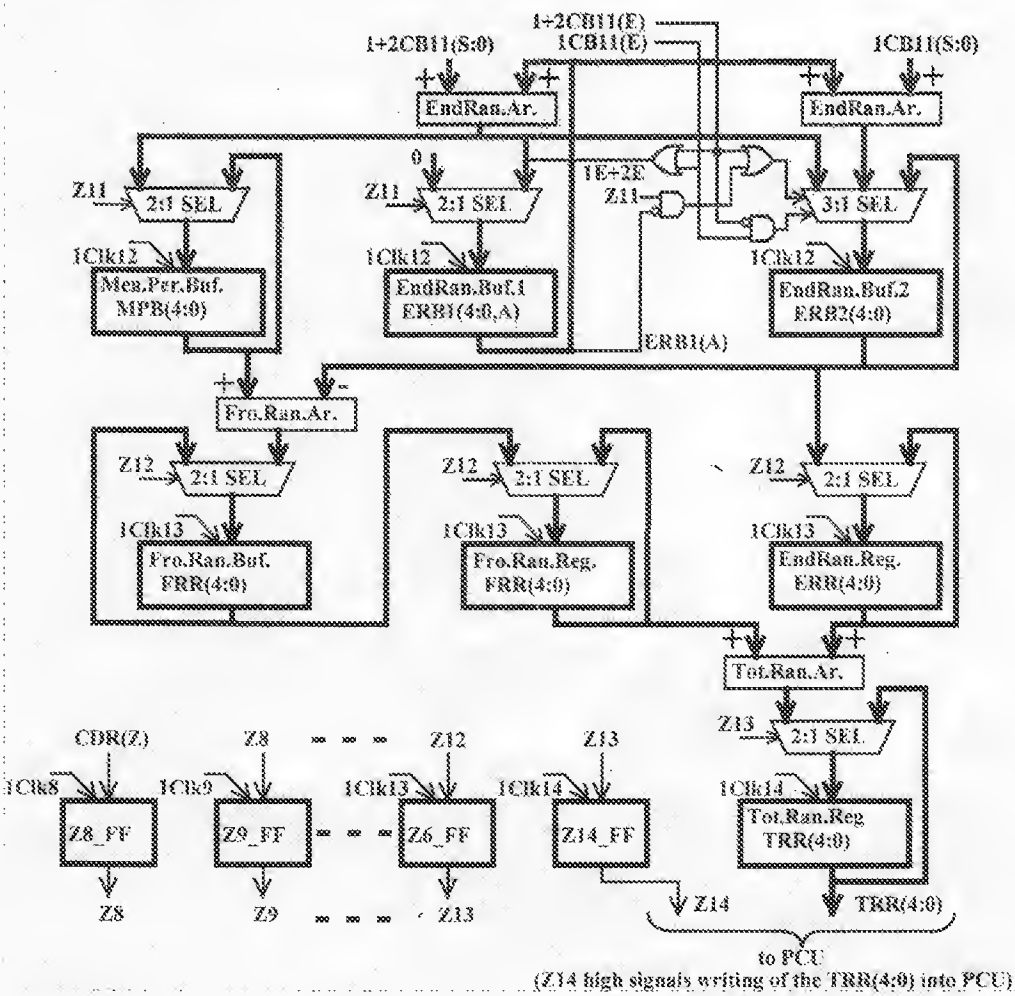


(DCR(Cf)/DCR(Cs) rising edge writes DCR(7:0)/DCR(15:8) accordingly into PCU Input Register)

FIG.3D Data Frequency Capturing



to PCU (CDR(Z) signals writing of the EDR(T:0) & CDR(4:0,A) into PCU)



(Z14 high signals writing of the TRR(4:0) into PCU)

FIG.4A Wave Form Screening & Capturing (WFSC)

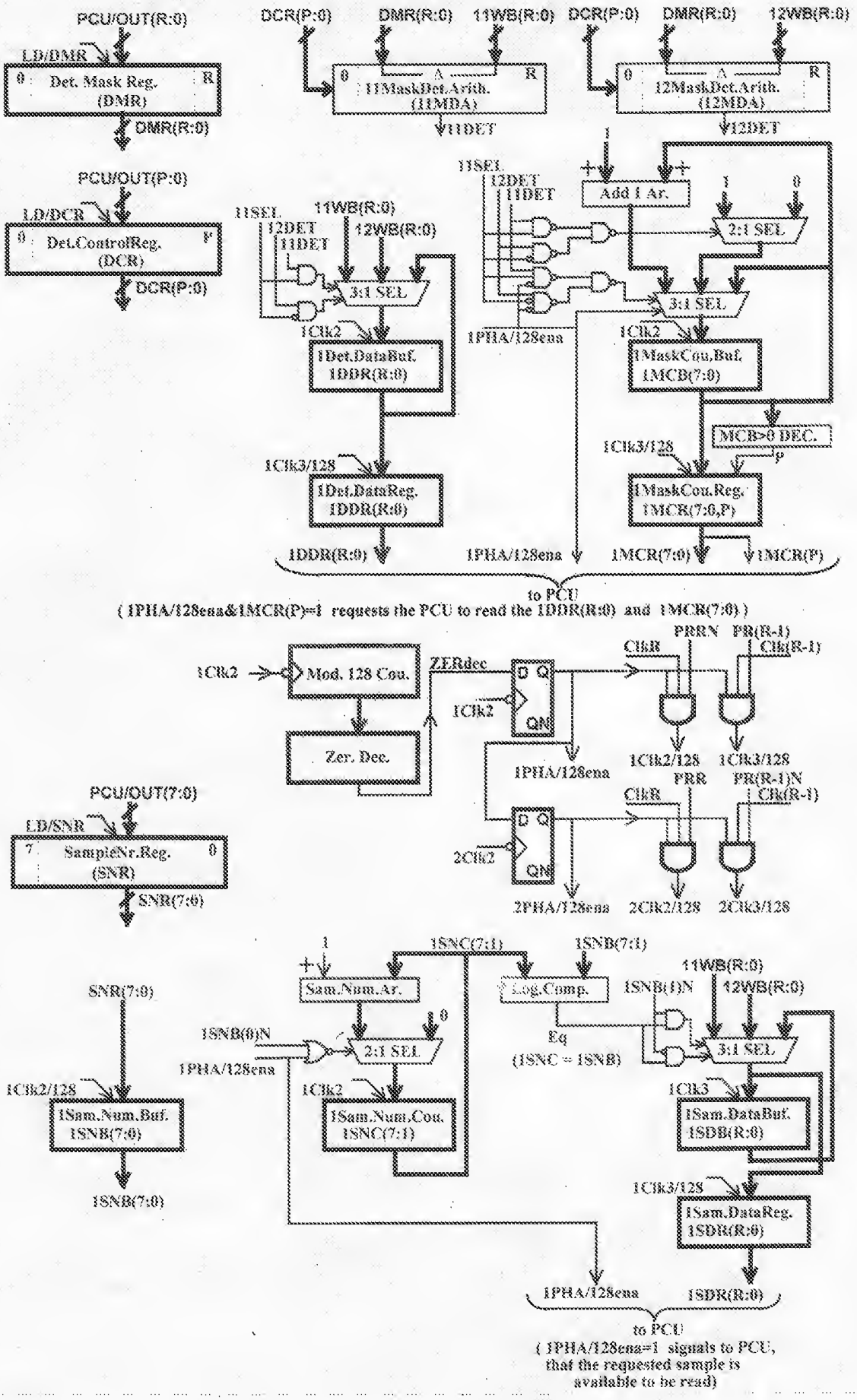


FIG.8 Timing Diagrams of the WFSC

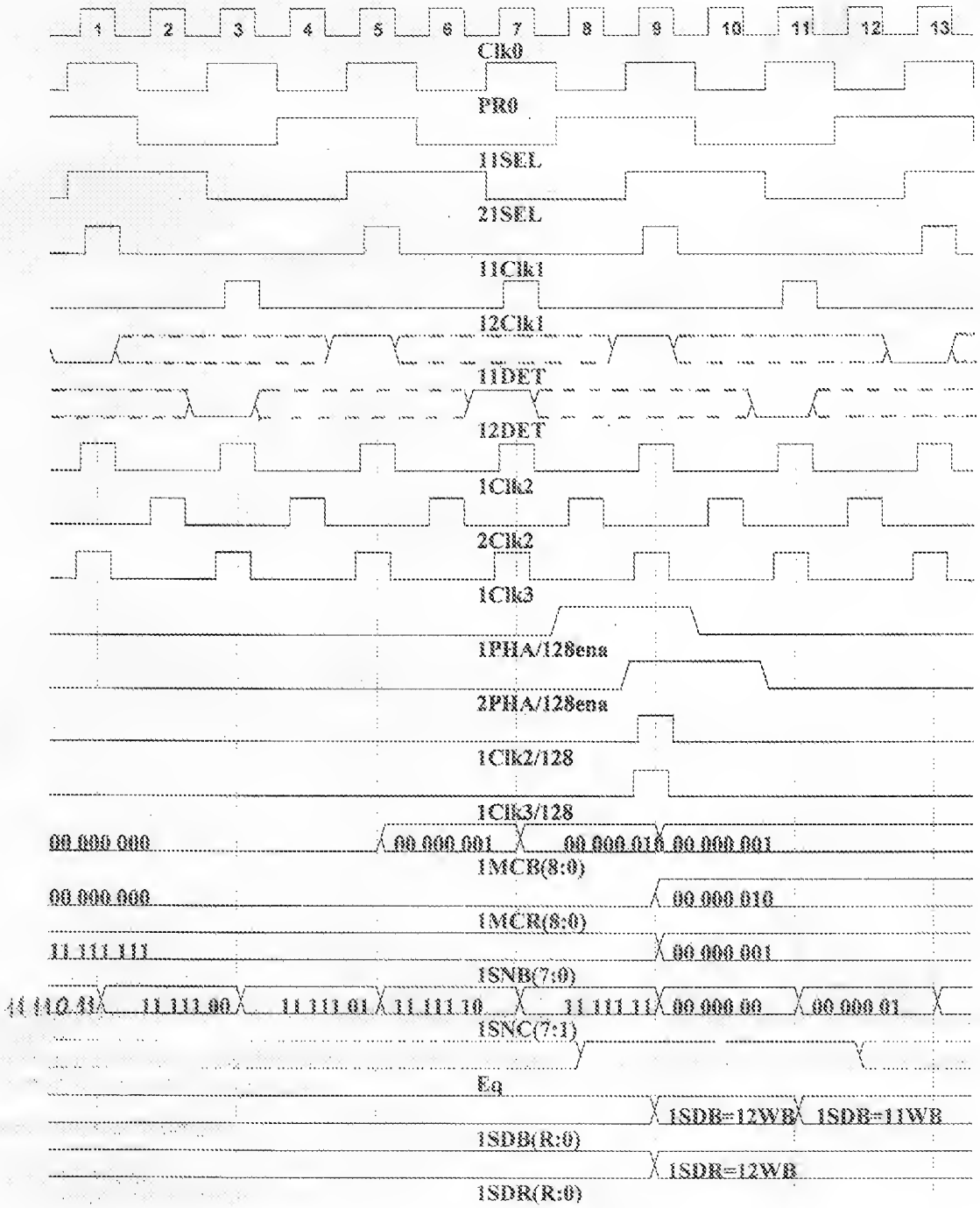


FIG.5 Wave Capturing including Edge Regions (WCER)

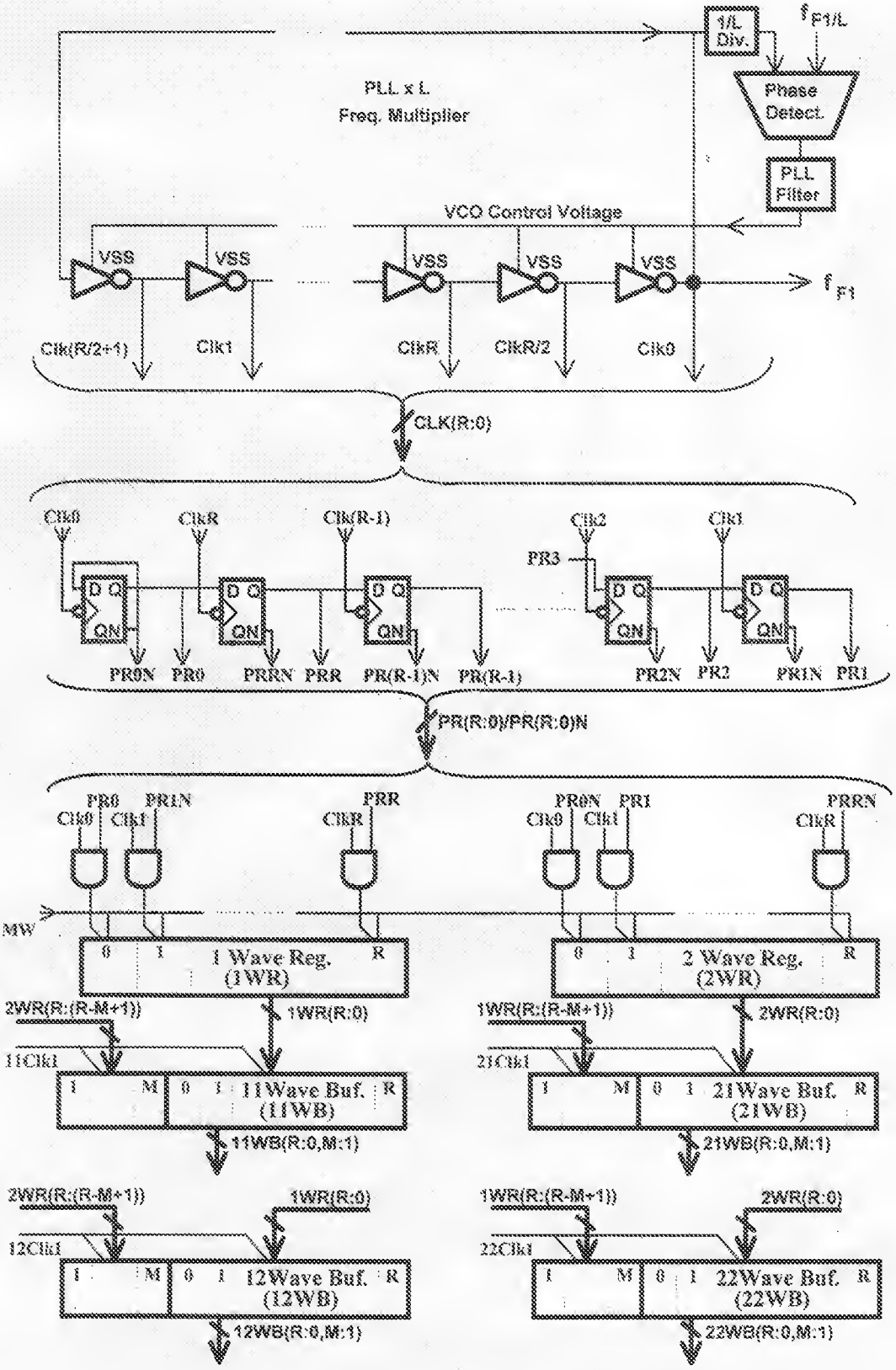
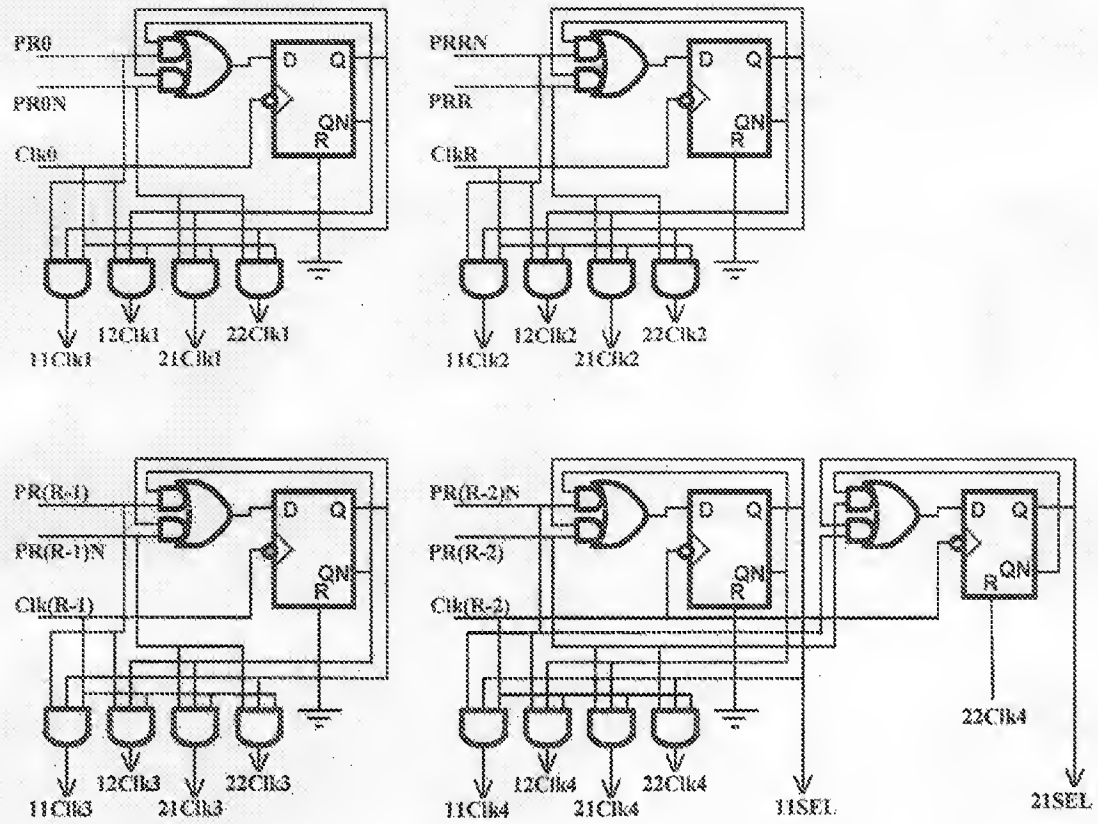
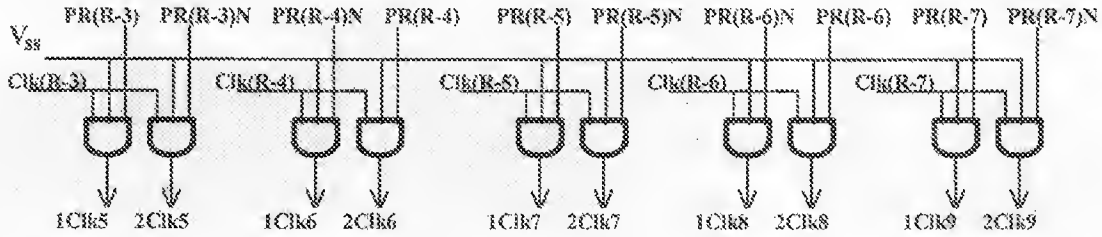


FIG.6 Sequential Clocks Generation for the NFED(SCG NFED)





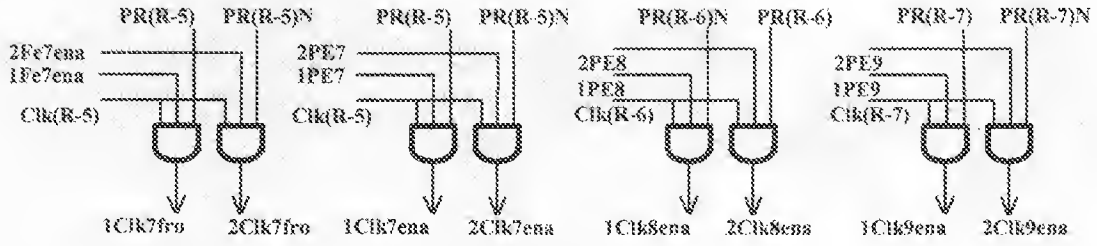


FIG.7 Noise Filtering Edge Detectors (NFED)